

# Quiz 1

(January 27<sup>th</sup> @ 5:30 pm)

## PROBLEM 1 (30 PTS)

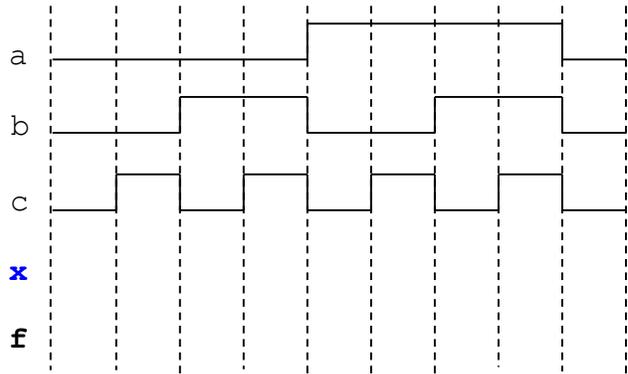
- Complete the timing diagram of the logic circuit whose VHDL description is shown below:

```

library ieee;
use ieee.std_logic_1164.all;

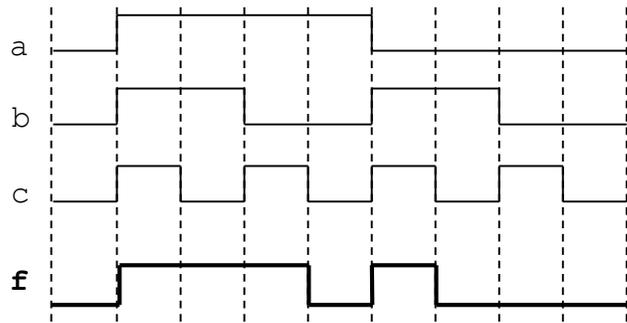
entity test is
    port ( a, b, c: in std_logic;
          f: out std_logic);
end test;

architecture struct of test is
    signal x: std_logic;
begin
    x <= a xor b;
    f <= x nand c;
end struct;
    
```



## PROBLEM 2 (40 PTS)

- The following is the timing diagram of a logic circuit with three inputs. Simplify the Boolean expression of the circuit and sketch the minimized circuit.



## PROBLEM 3 (30 PTS)

- Complete the timing diagram of the digital circuit shown below. You must consider the propagation delays. Assume the propagation delay of every gate is 5 ns. The initial values of all signals are plotted in the figure.

